MULTI-BANK MEMORY

Technical Field of the Invention

The present invention relates generally to memory devices, and in particular, the present invention relates to memory devices having multiple banks.

Background of the Invention

Direct Rambus Dynamic Random Access Memories, hereinafter referred to as DRDRAMs, are very fast, highly pipelined memory devices that are becoming an industry standard in high speed processing systems. DRDRAMs include a considerable amount of internal circuitry that supports the pipelined architecture so as to provide for very high communication bandwidths at the device boundary. DRDRAM sustained data transfer rates exceed 1 GB/s.

DRDRAMs, like most commercially available memories, include memory cells that are arranged in rows and columns. Unlike many commercially available memories, however, DRDRAMs are multi-bank devices that have memory cells logically arranged into banks that can be independently accessed. This results in multiple banks within each DRDRAM, each including a number of memory cells. Gathering the memory cells into banks, and allowing different banks to undergo separate operations simultaneously, increases the overall data transfer rate of the device.

Each bank is associated with one or more sense amplifiers that function to read data from, and write data to, the memory cells within the bank. The sense amplifiers serve as a data communications bridge between the banks of memory cells and the data buses external to the device. Banks are separately activated, possibly simultaneously, or overlapping in time, prior to a read or write operation. When a bank is activated, it communicates with one or more sense amplifiers. When the read or write operation is complete, the bank is deactivated, and the sense amplifiers are precharged, which readies the sense amplifiers for another operation.

Examples of DRDRAMs are described in: "Rambus Direct RDRAM 128/144-Mbit (256kx16/18x32s) Preliminary Information," Document DL0059, V1.11, June 2000; and "Rambus Direct RDRAM 256/288-Mbit (1Mx16/18x16d) Preliminary Information," Document DL0105, V1.1, August 2000. The contents of the aforementioned documents are hereby incorporated by reference.

Figure 1 shows a prior art multi-bank memory device. Memory device 100 includes memory cells arranged in rows and columns. Each column is shown as a vertical strip of memory cells, and each row is shown as a horizontal strip of memory cells. For example, strip 102 is a column that includes memory cells 120, 124, and 128, and strip 104 is a column that includes memory cells 130, 134, and 138. In memory device 100, each column corresponds to a single bank of memory cores. For example, memory cores 120, 124, and 128 of strip 102 are part of Bank 0, and memory cores 130, 134, and 136 of strip 104 are part of Bank 1. As shown in Figure 1, memory device 100 is arranged into "n" banks labeled Bank 0 through Bank (n-1).

Each bank shares sense amplifiers with at least one other bank. For example, sense amplifiers 140, 142, and 144 are shared between memory cores in Bank 0 and memory cores in Bank 1, and sense amplifiers 146, 148, and 150 are shared between memory cores in Bank 1 and memory cores in Bank 2.

Local row decoders are arranged within the array of memory cores. Each local row decoder provides wordline addressing to memory cores in close proximity. For example, in Figure 1, each of row decoders 122 and 126 provide row decoding for one or more of the memory cores in strip 102.

Column decoding, in contrast to row decoding, is performed globally. Column decode lines driven by column decoders typically traverse an entire row of memory cores, rather than only memory cores nearby. For example, column decoder 110 drives column decode lines 160 shown schematically in Figure 1 as an arrow. One or more of column decode lines 160 traverse multiple memory cells of the row to enable sense amplifiers within the row across from the column decoder. For example, a column decode line that enables sense amplifiers 146 to read from memory core 131 in Bank 2

will typically travel over, under, or past memory cores 120 and 130 from Banks 0 and 1, respectively.

In memory devices that allow simultaneous access to multiple banks, such as DRDRAMs, column decode lines that traverse memory cores from multiple banks can be problematic, in part because column decode lines addressed to one bank can cause electrical noise in memory cores of other banks being accessed. If noise is great enough, data errors can result.

sub a1 > Figure 2 shows a prior art sense amplifier suitable for use in a multi-bank memory. Sense amplifier 200 includes N-sense amplifier 202 and P-sense amplifier 204 coupled between sense nodes 232 and 234, isolation transistors 206 and 208, column decode transistors 210 and 212, and bank select transistors 216 and 218. Sense nodes 232 and 234 are coupled to input output (I/O) lines 224 and 222 through the column decode and bank select transistors. A column decode signal (Y-GATE) on node 214 is coupled to column decode transistors 210 and 212, and a bank select signal (BANK) on node 220 is coupled to bank select transistors 216 and 218. Other column decode lines 230 driven by the column decoder 110 (Figure 1) pass nearby sense amplifier 200. Other column decode lines 230 are coupled to other sense amplifiers (not shown) in the same manner that Y-GATE is coupled to sense amplifier 200 on node 214.

sub a2 > The operation of sense amplifier 200 is well known. When data from a memory core either to the left or right of sense amplifier 200 is to be read, the appropriate isolation transistors are turned on, and the N-sense and P-sense amplifiers are activated. The data value (and its complement) being read appears on sense nodes 232 and 234. When both the column decode signal (Y-GATE) on node 214 and the bank select signal (BANK) on node 220 are asserted, transistors 210, 212, 216, and 218 turn on and couple sense amplifier 200 to I/O lines 222 and 224.

When sense amplifier 200 is used in a multi-bank memory device that allows simultaneous operations among banks, the other column decode lines 230 can be actively changing during the operation of sense amplifier 200, causing noise that can potentially cause a data error. For example, referring now back to Figure 1, if sense

amplifier 140 is sensing data from memory core 120 in bank 0 while a column decode line addressing sense amplifier 146 is changing, a data error in sense amplifier 140 can result. As memory devices become larger, and more banks are added, the problem becomes worse.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternate multi-bank memory devices.

Summary of the Invention

The above mentioned problems and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

In one embodiment, a memory device includes a plurality of banks, each including a plurality of memory cores, and also includes a plurality of sense amplifiers shared among memory cores of different ones of the plurality of banks. The memory cores from two of the different ones of the plurality of banks are interleaved in a strip with the plurality of shared sense amplifiers.

In another embodiment, an integrated circuit includes an array of memory cores having a first dimension and a second dimension, where a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank. In this embodiment, a plurality of sense amplifiers are arranged between memory cores from the first bank and memory cores from the second bank.

In another embodiment, a computer system includes a processor and a memory device coupled to the processor. The memory device includes a plurality of rows and columns of memory cores, and also includes a plurality of sense amplifiers positioned between memory cores within each row, wherein every other memory core within each row is assigned to a bank.

Brief Description of the Drawings

Figure 1 is a diagram of a prior art multi-bank memory device.

Figure 2 is a diagram of a prior art sense amplifier.

Figure 3 is a diagram of a multi-bank memory device of the present invention.

Figure 4 is a diagram of a sense amplifier in accordance with the present invention.

Figure 5 is a diagram of a processing system in accordance with the present invention.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Figure 3 shows a multi-bank memory device in accordance with the present invention. Memory device 300 includes memory cells arranged in rows and columns. Each column is shown as a vertical strip of memory cells, and each row is shown as a horizontal strip of memory cells. For example, strip 302 is a column that includes memory cells 320, 324, and 328, and strip 370 is a row that includes memory cells 320 and 330. As shown in Figure 1, memory device 100 is arranged into "n" banks labeled Bank 0 through Bank (n-1).

Each row in memory device 300 includes memory cores from two banks interleaved together. For example, strip 370 includes memory cores from Bank 0 and Bank 1 alternating across the strip. Also for example, strip 372 includes memory cores from Bank 2 interleaved with memory cores from Bank 3.

Each row includes sense amplifiers that are shared between two banks of memory cores. For example, sense amplifiers 340 and 346 are shared between memory cores in Bank 0 and memory cores in Bank 1, and sense amplifiers 342 and 348 are shared between memory cores in Bank 2 and memory cores in Bank 3.

Local row decoders are arranged within the array of memory cores. Each local row decoder provides wordline addressing to memory cores in close proximity. For example, in Figure 3, each of row decoders 322 and 326 provide row decoding for one or more of the memory cores in strip 302. In some embodiments, row decoders are shared among multiple memory cores, with latches and row drivers dedicated to each bank. For example, in the embodiment of Figure 3, row decoders can be shared between Bank 0 and Bank 2. In operation, each of these row decoders performs a row decode operation, and the result is steered into a latch for Bank 0 or a latch for Bank 2.

Column decode lines driven by column decoders typically traverse an entire row of memory cores, rather than only memory cores nearby. For example, column decoder 310 drives column decode lines 360 shown schematically in Figure 3 as an arrow. One or more of column decode lines 360 traverse multiple memory cells of the row to enable sense amplifiers within the row across from the column decoder. For example, a column decode line that enables sense amplifiers 346 to read from memory core 331 in Bank 0 will typically travel over, under, or past memory cores 320 and 330 from Banks 0 and 1, respectively.

Multi-bank memory device 300 is useful in part because each row includes memory cores from banks that cannot be simultaneously accessed. For example, memory cores from Bank 0 and Bank 1 are interleaved in a single row. Because memory cores from Bank 0 and Bank 1 share sense amplifiers, they cannot be simultaneously accessed. Banks in other rows, however, may be accessed at the same time or overlapping in time with an access of memory cores in Bank 0 or Bank 1. Each row has at least one column decoder dedicated thereto. For example, row 370 has column decoder 310 dedicated thereto. Because each row supports only one access at a time, column decode lines driven by each column decoder change only during an access

to that particular row, and the noise problem associated with memory device 100 (Figure 1) is avoided.

Multi-bank memory device 300 is arranged as a two dimensional array of memory cores. One dimension of the array includes strips of memory cores, each strip having interleaved memory cores from two separate banks. The other dimension of the array contains strips that do not include memory cores from common banks. In the embodiment shown in Figure 3, each strip that includes interleaved memory cores from two banks is situated in a a row, and strips that do not include memory cores from common banks are situated in columns. In other embodiments, columns include interleaved memory cores rather than rows.

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Figure 4 shows a sense amplifier in accordance with the present invention. Sense amplifier 400 includes N-sense amplifier 402 and P-sense amplifier 404 coupled between sense nodes 432 and 434, isolation transistors 406 and 408, and column decode transistors 410 and 412. Sense nodes 432 and 434 are coupled to input output (I/O) lines 424 and 422 through the column decode transistors. A column decode signal (Y-GATE) on node 414 is coupled to column decode transistors 410 and 412.

Other column decode lines 430 driven by the column decoder pass nearby sense amplifier 400. Other column decode lines 430 are coupled to other sense amplifiers (not shown) in the same manner that Y-GATE is coupled to sense amplifier 400 on node 414. Because each row includes interleaved memory cores from two banks, the sense amplifiers in the same row as sense amplifier 400 access memory cores from the same two banks as sense amplifier 400. As a result, other column decode lines 430 are not changing when sense amplifier 400 is sensing.

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In operation, when data from a memory core either to the left or right of sense amplifier 400 is to be read, the appropriate isolation transistors are turned on, and the N-sense and P-sense amplifiers are activated. The data value (and its complement) being read appears on sense nodes 432 and 434. When the column decode signal (Y-GATE) on node 414 is asserted, transistors 410 and 412 turn on and couple sense amplifier 400 to I/O lines 422 and 424.

Sense amplifier 400 does not include bank select transistors such as bank select transistors 216 and 218 (Figure 2). This is because each row only includes memory cores from two banks that cannot be simultaneously accessed, and there is no need to identify which bank is being accessed with a bank decode signal. As a result, sense amplifier 400 can be made significantly smaller than sense amplifier 200 (Figure 2).

Node 414 and other column decode lines 430 are conductors that run substantially parallel to a row of memory cores and sense amplifiers. For example, referring now back to Figure 3, column decode lines 160 run substantially parallel to row 370. The conductors can be made from metal, poly, or any other suitable material. For example, in a two-layer metal process, the column decode lines can be dedicated to a single metal layer. Also for example, in a single layer metal process, the column decode lines can be buried on poly layers.

Figure 5 is a diagram of a processing system in accordance with the present invention. System 500 includes processor 505 and memory device 510. Memory device 510 includes memory array 515, address circuitry 520, and read circuitry 530, and is coupled to processor 505 by address bus 535, data bus 540, and control bus 545. Memory array 515 includes memory cells and circuits arranged in accordance with those embodiments discussed above with reference to Figures 3 and 4.

Memory device 510 is typically mounted on a motherboard. Processor 505, through address bus 535, data bus 540, and control bus 545 communicates with memory device 510. In a read operation initiated by processor 505, address information, data information, and control information are provided to memory device 510 through busses 535, 540, and 545. This information is decoded by addressing circuitry 520 and read circuitry 530. Successful completion of the read operation results in information from memory array 515 being communicated to processor 505 over data bus 540.

Conclusion

A multi-bank memory device has been described that includes rows and columns of memory cores. Each row includes memory cores from one bank interleaved

with memory cores from another bank. Banks in different rows can be simultaneously accessed without noise coupling from one access to the other.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.